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Design of Decompressor Using Cumulating Transmission Cyclic Shift Updating Compression Technique for Multiple Scan Chains

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Abstract : In VLSI designs, the circuits are designed and then tested using DFT(Design for Testability) approach. Overall testability of the circuit can be improved using structured DFT. The difficulty to observe and control the internal state of the circuit is one of the major problems in testing a sequential circuit. Use of Scan based testing approach overcomes this problem. In addition to reduction in test time, scan based test approach increases the number of input channels, hardware required and even results in lesser coverage of faults. Reducing the amount of test data, has the advantage of reduction in memory required and even the test time required, as lesser is the data to be transferred. This is achieved through a compression technique which uses cyclic shift. This method increases the correlation between the reference input and test inputs with the use of don't bits. In this paper, a decompression scheme is proposed for the above technique, which helps in retrieving the original test data efficiently.

Keywords: Multiple scan chain; cyclic shift; decompression.

1. INTRODUCTION

In an automatic test equipment (ATE), due to advancements in design technologies, there is a need for higher volume of test data but limited memory and I/O Channels are present. Various multiple scan chain designs are proposed in order to speed up the testing process. The compression techniques can be categorized based on the presence or absence of LFSR circuit, which necessitates the use of polynomial compression schemes, as LFSR coding and non-LFSR coding [1]. Other type is based on the connectivity between the input multiple scan chains and external input channels which is topology based. In coding based schemes, the compression ratio is higher but at the cost of increased input channels. The other scheme might reduce the required channels but in turn increase the required interconnection which in turn increases the hardware overhead.

Achieving ideal data compression ratio is difficult, in spite of implementation of multiple scan chain design. Don't care bits are the one whose value is not assigned during ATPG. As the faults are structurally related in the circuit, their values can be useful for correlation. Before being shifted into the scan chain, Original test vectors are got back by the expansion of compressed stimulus by a decompressor [2].

If the numbers of registers in the circuit are increased, the input channels required can be reduced. Best compression effect and lesser number of shift registers is a trade-off to be targeted. Higher compression effects are observed in cyclic shift compression technique as Don't care bits are used to check for compatibility and inverse compatibility between vectors [3]. This technique overcomes the disadvantages of the earlier methods. Proper decompression solution is proposed for this scheme.

In this paper, an architecture is proposed for decompressing the test inputs. The compressed

datas stored in memory is decompressed and fed to the DuT(Design under Test) and correctness is observed. Section 2 explains the proposed design which includes a FSM(Finite State Machine). Section 3 gives the results and section 4 is the conclusion.

2. PROPOSED DESIGN

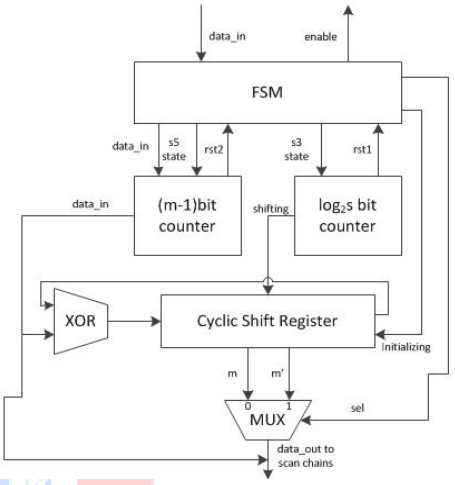
The knowledge of core internal information of the circuit is not required for implementing the compression technique as the IP core vendors provide the required test vectors [1]. Two vectors which are neither compatible nor inverse compatible can be correlated through cyclic shift technique. An illustration is shown below. Consider the vectors v1=0XX10011 and v2=0110XXXX, after t=cyclic right shift of vector v1, v3=0110XX10 which is compatible with vector v2. The advantage of the above scheme is use of don't bits which helps in achieving higher compression efficiency with the increased correlation between the vectors. Cyclic shift is implemented through the use of Shift register.

Cumulating Transmission Cyclic Shift Updating(CDCS) Compression Technique is explained below. Within a maximum of 's' shifts, the input vector is matched with the data in the reference vector and is then applied to the scan chains. An identifier '0' signifies compatibility and '1' signifies the inverse compatibility. Identifier '11' followed by '0' or '1' indicates that there is a shift or two and the last bit signifies the relation between them. The special case of neither compatible nor inverse compatible is indicated by '100' identifier. The code word and identifier are made use of in decompression [4].

The decompressor scheme is proposed for the above technique as shown in figure 1. It is a sequential design consisting of a Cyclic Shift Register(CSR), Finite State Machine(FSM), Counters, Multiplexer and a XOR logic.

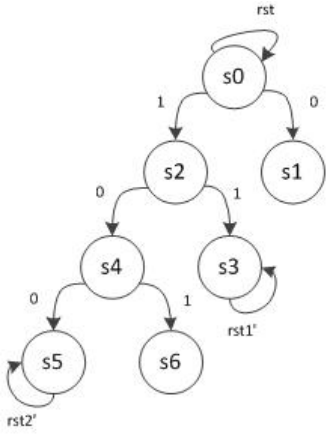
Bit interleaving technique is used and data is fed bit-wise to the FSM. It has 6 states based on the received bits. If the received bit is '0', output is directly taken from the CSR as the vectors are Compatible. If '1' is received, negation of contents of CSR is taken. In case 's' shifts have taken place (max value of s is taken to be two), the counters come into picture. $\log_2$S counter is used for shifting the contents of CSR. If the case is of neither compatible nor inverse compatible, XOR logic is used to perform modulo-2 addition of received vector and reference vector and contents in the CSR get shifted and updated.

Figure 1. Architecture Of Decompressor



The input vector gets decoded based in the identifier which happens to be the last bit in this case. The finite state machine indicating this operation is shown in Figure 2.

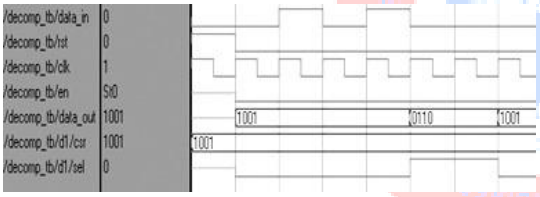
Fig 2:Finite State Machine



3. EXPERIMENTAL RESULTS

The verilog file (.v file) is simulated in Cadence nclaunch tool and the change of states in the design with respect to the input identifiers and select lines is shown in figure 3. The Cyclic Shift Register(CSR) has been initialized to 1001 value. Here the simulation starts with data_in=0 value. According to the decompression FSM whenever input is 0, by assigning 'sel' as 0 the shift register value CSR as such is fed to output scan chains. Following, the input 'data_in' changes to 1 then 0 and 1. Whenever an input combination of 101 comes, 'sel' control is made 1 and inverted output from shift register is fed to scan chains. therefore data_out will become 0110. Further data_in=0 and 1001 output is taken from shift register CSR. Likewise, for the other cases such as 11 and 100, FSM changes its states, and the corresponding output is fed to 'data_out'.

Figure 3. Simulation Result



Using Cadence rc tool, the design is synthesized in 0.18µm CMOS technology utilizing a full-custom design approach and scalable design rules. The synthesize step is carried out using 'slow.lib' library file of 0.18µm technology and thus obtained a power of 0.035mW. Further reduction of power to 0.017mW is achieved after adding the low power constraints.

4. CONCLUSION

In the proposed decompressor design, it is observed that there is a reduction in dynamic power consumption after the addition of low power constraints. Upto 50% reduction is achieved. Only one input channel is required for data. Thus a simple, low power, area efficient decompressor design is proposed.

5. REFERENCES

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