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DIRECT DIGITAL SYNTHESIS TECHNIQUE BASED RF-EXCITER CARD FOR WIND PROFILING APPLICATION

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ABSTRACT
With the advancement of semiconductor manufacturing processes and the introduction of Field Programmable Gate Array (FPGA) and Digital Signal Processors (DSPs) to the consumer market, the usage of Digital technique has become a popular approach for synthesizing complex RF waveforms for wind profiler applications. Wind profilers, operating in 48-52 MHz band, are air radars used to estimate horizontal and vertical wind velocities up to a height of 20 Kms. They are used for providing wind velocity data for aircrafts and launch vehicles.
The RF Exciter card used for wind profiler radars would employ pulsed, barker coded VHF waveform. The Exciter card being designed has to generate frequencies in the range 48-52MHz by using DDS chips. In addition to this, the card has to generate the stable Local oscillator [STALO] frequency of 35MHz, for down conversion of the received signal and 64 MHz ADC clock for digitizing the received signal. Xilinx FPGA is used to program the 3 DDS chips using SPI, apart from generating the control signals and barker code for modulation.

Keywords
Direct Digital Synthesizer, FPGA, SPI, Radar waveform generator, Frequency Tuning Word.

1. INTRODUCTION
Wind profilers are used for providing wind velocity data for aircrafts. In 1990, the National Aeronautic and Space Administration/ Kennedy Space Centre (NASA/KSC) installed a 50-MHz Doppler radar wind profiler (DRWP) to evaluate its applicability for measuring upper-level winds in support of space lift operations [1]. Wind profilers can measure winds many kilometres from the ground and they sample winds almost continuously. The Doppler frequency content of the signal returning from the atmosphere is extracted in order to estimate the wind velocities. The winds are measured nearly directly above the site and both the horizontal and vertical air velocity can be measured by transmitting the radar pulses along each of the antenna's pointing directions. The duration of a pulse determines its length and the volume of air illuminated. Small amounts of the energy are scattered back towards the radar. Delays of fixed intervals are built into data processing system, so that the radar receives scattered energy from discrete altitudes, referred to as range gates. The Doppler frequency shift of the backscattered energy is determined, and then used to calculate velocities of air toward or away from radar along each beam as a function of altitude. The source of the backscattered energy is the small-scale turbulent fluctuations that will induce irregularities in the refractive index of the atmosphere at radar frequencies. The source of the backscattered energy is small-scale turbulent fluctuations that induce irregularities in the refractive index of the atmosphere at radar frequencies. The fundamental assumption is that these irregularities move with the wind. The radar is most sensitive to scattering by turbulent eddies in density and water vapour whose spatial scale is ½ the wavelength of the radar. The fundamental process upon which Doppler systems are based is the frequency shift of a signal seen by an observer when the source of the signal is approaching or receding. For electromagnetic signals,

$$fd = f(1+2\ v/c) \qquad (1)$$

where *fd* is the Doppler shifted frequency, *f* is the frequency of the source, *v* is the radial velocity relative to the observer (positive for motion toward the observer and negative for motion away), and *c* is the speed of light.

1.1 Radar waveform generators
The wind profiler transmits the radar pulse to determine the wind velocities; in this section various methods employed to generate the radar signals are briefly discussed. Post the World War II immense research was done in the development of radar system. Earlier in weather radars the vacuum tube technology was employed to generate radars, some of the technology used were the magnetron, klystron, travelling wave tubes techniques.

With further advancement in this field radar waveforms can be generated using two approaches, namely (i) the analog microwave circuit approach, or (ii) the digital approach. In the analog microwave circuit approach, a Voltage Controlled Oscillator (VCO) is used [2] where the output frequency of the VCO is adjustable by changing the applied tuning voltage.

The drawback for analog approach is that, VCOs readily available in the market have limited frequency sweep rate (frequency settling time), which is in the range of milliseconds. In modern radar system, the digital approach is the preferred choice due to the fact that digital electronics offer better stability, repeatability, and flexibility over an equivalent analogue approach [3].

With the advancement of semiconductor manufacturing process (22nm in 2011), and the introduction of Field Programmable Gate Array (FPGA) and Digital Signal Processors (DSPs) to the consumer market, the technique of Direct Digital Synthesis (DDS) has become a popular approach for synthesizing complex RF waveforms for application in radar and communication systems.

2. PROPOSED SYSTEM ARCHITECTURE

The RF Exciter card used for wind profiler radars would employ pulsed, barker coded VHF waveform. The Exciter card has to generate frequencies in the range 48-52 MHz by phase locking to an external 10MHz rubidium source. The 10 MHz clock, provided externally from a Rubidium source has to serve as the locking frequency for all the frequencies generated by the board. So a clock divider AD9520 is used for distributing the 10 MHz clock to 3 DDS Chips.

The clock divider has an on board PLL (phase locked loop) that will multiply the 10 MHz clock to 1 GHz and is fed to the three DDS chips AD9910. DDS chip is used to generate the VHF frequency. The card has to generate the stable Local oscillator [STALO] frequency-35MHz, for down conversion of the received signal. In addition to this, the card also has to generate 64 MHz ADC clock for digitizing the received signal.

Xilinx FPGA is used to program the three DDS chips using SPI. The proposed system block diagram for the DDS based RF exciter card is as shown in Fig 2.1. The main blocks of the RF exciter card consists of (i) clock divider (ii) three DDS chips and (iii) the FPGA.

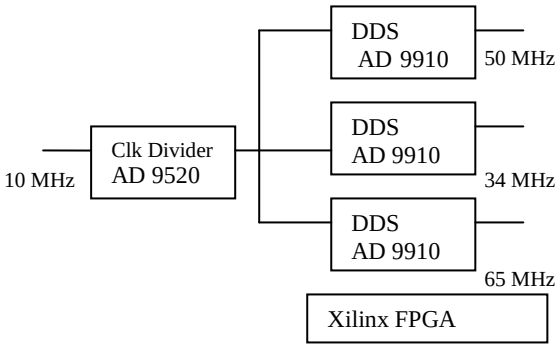

Fig 2.1: Proposed Block Diagram of DDS based RF Exciter

2.1 Clock Divider AD9520

The AD9520 provides a multi-output clock distribution function with sub-picosecond jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 2.53 GHz to 2.95 GHz.

The AD9520 serial interface supports both SPI and I2C ports. An in-package EEPROM can be programmed through the serial interface and store user-defined register settings for power-up and chip reset. The AD9520 supports output in four groups, and it operates on 3.3 V.

The AD9520 can be configured in several ways by configuring the control registers. The block diagram of AD 9520 is shown in Fig 2.2. When the desired configuration is programmed, the user can store these values in the on-board EEPROM to allow the part to power up in the desired configuration without user intervention. The clock divider AD9520 is used to multiply the 10 MHz external clock to 1 GHz by using the on board PLL multiplier which is fed to the DDS chip.

2.2 Direct Digital Synthesizer

Direct Digital Synthesizer is a type of the frequency synthesizer used for creating arbitrary RF waveforms from a single, fixed-

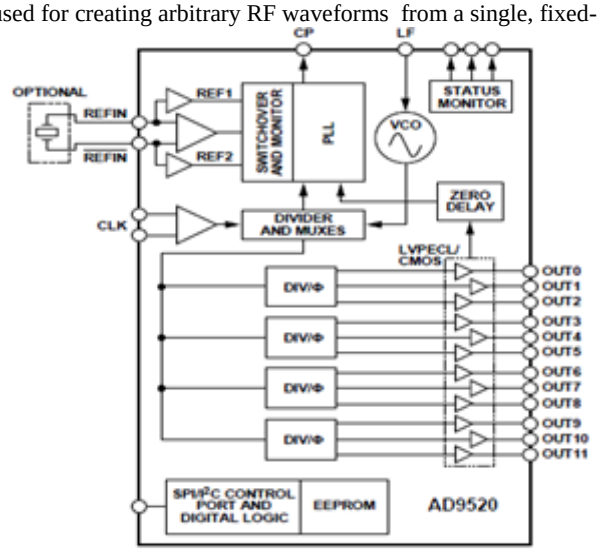

Fig 2.2: Block diagram of clock divider AD9520

frequency reference clock.The DDS operates on the principle of sampling theorem (Nyquist theorem). A basic Direct Digital Synthesizer consists of a frequency reference (often a crystal oscillator), a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC) as shown in Fig 2.3.

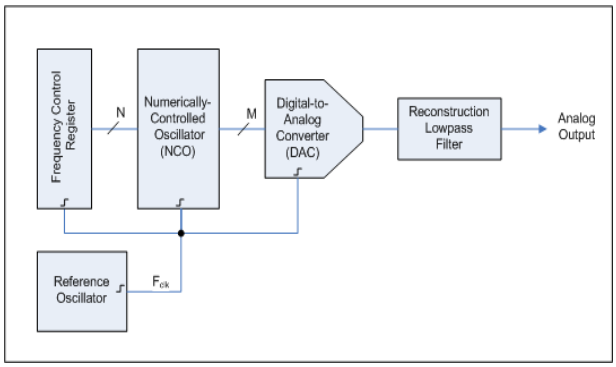

Fig 2.3: Basic DDS block diagram

The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the *NCO* which produces at its output a discrete-time, quantized version of the desired output waveform (often a sinusoid) whose period is controlled by the digital word contained in the Frequency Control Register.

The sampled, digital waveform is converted to an analog waveform by the *DAC*. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process.

The AD9910 is a direct digital synthesizer (DDS) featuring an integrated 14-bit DAC and supporting sample rates up to 1 GSPS. The AD9910 employs an advanced, proprietary DDS technology that provides a significant reduction in power consumption without sacrificing performance. The DDS/DAC combination forms a digitally programmable, high frequency,

analog output synthesizer capable of generating a frequency agile sinusoidal waveform at frequencies up to 400 MHz. The user has access to the three signal control parameters that control the DDS: frequency, phase, and amplitude.

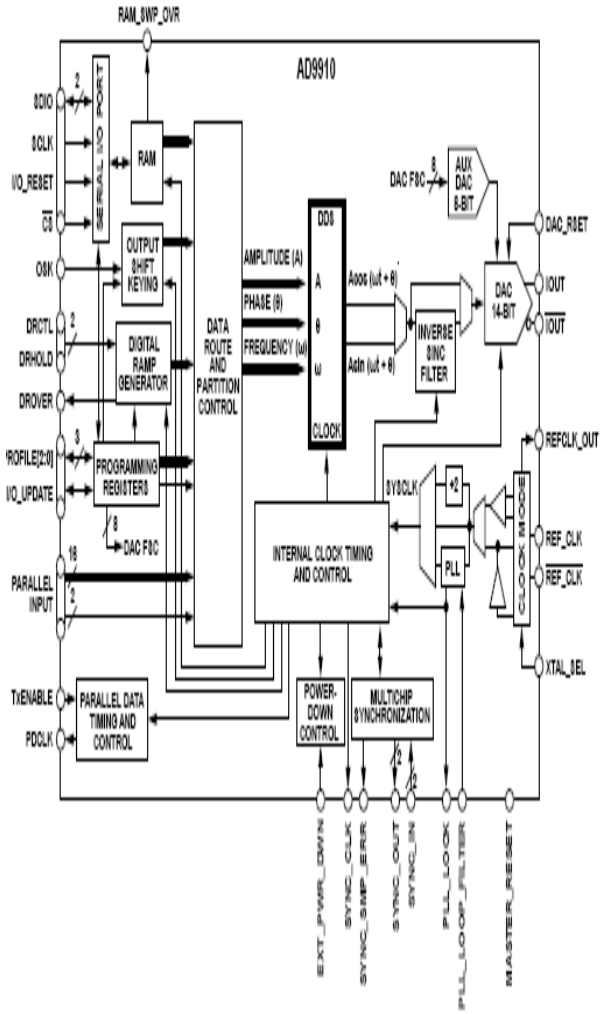

Fig 2.4: Block diagram of AD 9910 (from analog devices)

The DDS provides fast frequency hopping and frequency tuning resolution with its 32-bit accumulator. With a 1 GSPS sample rate, the tuning resolution is ~0.23 Hz. The DDS also enables fast phase and amplitude switching capability. The AD9910 is controlled by programming its internal control registers via a serial I/O port.

The AD9910 includes an integrated static RAM to support various combinations of frequency, phase, and/or amplitude modulation. The AD9910 also supports a user defined, digitally controlled, digital ramp mode of operation. In this mode, the frequency, phase, or amplitude can be varied linearly over time. For more advanced modulation functions, a high speed parallel data input port is included to enable direct frequency, phase, amplitude, or polar modulation. The block diagram of AD9910 is shown in Fig 2.4.

3. SYSTEM DESIGN

In a system, the different components are connected with each other and they are independent. Fig.3.1. depicts the block diagram of system design.

3.1 PC Interface

To enhance user convenience, we have developed a PC interface which allows the user to manipulate input parameters

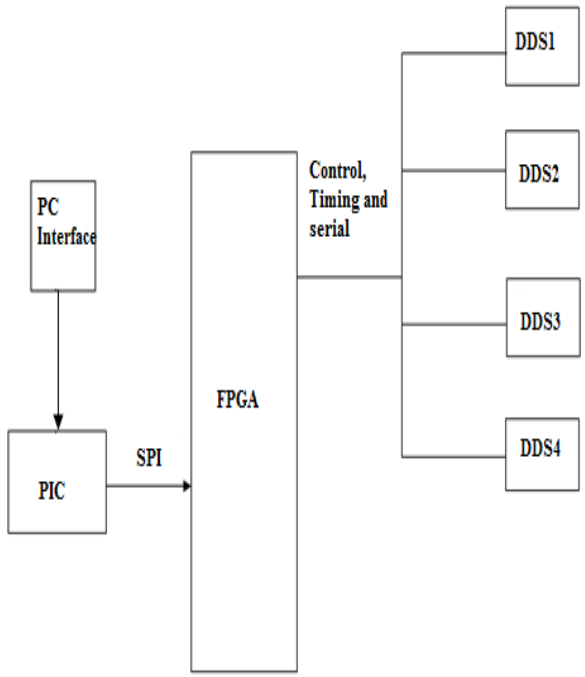

Fig 3.1: Block Diagram

of DDS chips. This GUI is design using Visual Basic 2010. The various DDS input parameters like phase, amplitude, frequency etc can be altered using this application resulting in the update of DDS registers. The updated register values are then finally sent to PIC microcontroller by using VB serial communication.

3.2 PIC Microcontroller

The microcontroller used is PIC microcontroller of version DsPIC33FJ256. It is 100-pin 16-bit low power, high speed CMOS FLASH/SRAM microcontroller. The microcontroller will receive the data from the PC interface through serial communication using UART. The data is sent to the FPGA through serial communication.

3.3 FPGA

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL). XC3S500E4FG320CSE family version is used. In this research project, it is used in order to control the multiple DDS chips.

3.4 Multi-Channel DDS Chips

Multichannel waveform generator can be implemented using multiple DDS chips and FPGA to control these DDS chips. FPGA is connected to PC through SPI. The DDS chips have

some common control lines, and some that are individual per channel. Multiple devices are synchronized when their clock states match.

4. WORKING PRINCIPLE

In this research project, the DDS technique is used for RF clock generator in order to generate multi-channel high speed, fine tuneable waveforms. The GUI designed using VB 2010 is used to interface the PC with the PIC microcontroller. The PIC microcontroller is used for the purpose of serial communication with the FPGA chip. We have 4 DDS channels which can operate at different frequencies simultaneously depending upon the input parameters entered at the GUI evaluation board.

Output frequency range of each DDS chip varies from 0 to 400MHz. In our project we need to generate a VHF frequency signals in the range of 48-52MHz. It also requires a stable local oscillator frequency of 32MHz for down conversion of received signal and a 64MHz signal to generate the ADC clock for digitizing the received signal.

5. IMPLEMENTATION

The multichannel radar waveforms can be implemented using multiple DDS chips. FPGA is used to control these DDS chips by using serial peripheral interface. FPGA is connected to PC through SPI. The DDS chips have some common control lines, and some that are individual per channel. We provide sysclk signal and SCLK signal from FPGA and are distributing these signals to all DDS chips by using AD9520. Here in order to synchronize the DDS chips we have to distribute SYNC_CLK from master DDS to all the other DDS chips this done by ADCLK846. The detailed block diagram is as shown in Fig 3. An external clock of 10 MHz is provided from a rubidium source this is fed to the AD 9520 clock divider.

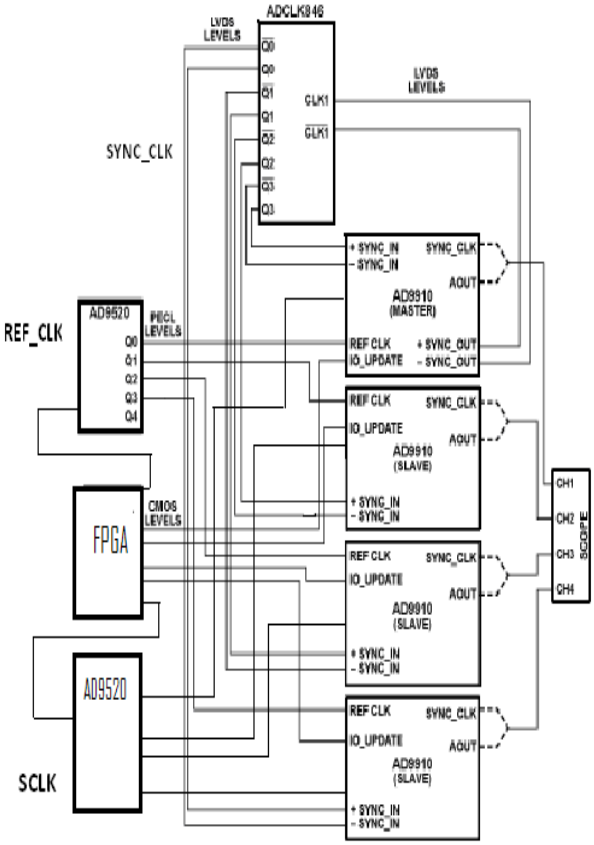

Fig 5.1: Detailed block diagram of the RF card

The AD 9520 has on board phase multiplier and SPI interface through which the chip is configured to generate 1 GHz signal by phase locking it to the external clock. The 1 GHz signals are fed to the DDS chips. The DDS chip AD 9910 is configured through FPGA by SPI, The AD9910 is operated in the single tone mode where the amplitude, frequency and phase can be configured to generate the desired frequency waveform. The DDS chip AD9910 is configured through FPGA by SPI, The AD9910 is operated in the single tone mode where the amplitude, frequency and phase can be configured to generate the desired frequency waveform. The output frequency (f_{OUT}) of the AD9910 is controlled by the frequency tuning word (FTW) at the frequency control input to the DDS. The relationship among f_{OUT}, FTW, and f_{SYSCLK} is given by

$$\text{fout} = \left(\frac{\text{FTW}}{2^{32}}\right) \text{fsysclk} \qquad (2)$$

where FTW is a 32-bit integer ranging in value from 0 to 2,147,483,647 (231 − 1), which represents the lower half of the full 32-bit range. This range constitutes frequencies from dc to Nyquist (that is, ½ f_{SYSCLK}).The relative phase of the DDS signal can be digitally controlled by means of a 16-bit phase offset word (POW). The phase offset is applied prior to the angle-to-amplitude conversion block internal to the DDS core. The relative phase offset ($\Delta\theta$) is given by

$$\theta = 2\pi \left(\frac{\text{POW}}{2^{16}}\right) \qquad (3)$$

where the upper quantity is for the phase offset expressed as radian units and the lower quantity as degrees. To find the POW

value necessary to develop an arbitrary Δθ, solve the previous equation for POW and round the result (in a manner similar to that described previously for finding an arbitrary FTW).The relative amplitude of the DDS signal can be digitally scaled (relative to full scale) by means of a 14-bit amplitude scale factor (ASF). The amplitude scale value is applied at the output of the angle-to-amplitude conversion block internal to the DDS core. The amplitude scale is given by

$$\text{Amplitude Scale} = \frac{\text{ASF}}{2^{14}} \qquad (4)$$

where the upper quantity is amplitude expressed as a fraction of full scale and the lower quantity is expressed in decibels relative to full scale. To find the ASF value necessary for a particular scale factor, solve equation 3 for ASF and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

6. HARDWARE IMPLEMENTATION

The PCB board shown in Fig.6.1 consists of XILINX FPGA and the PIC microcontroller. The PCB has a serial port availability. The FPGA version used is XC3S500E4FG320CSE. The PIC microcontroller used belongs to the dsPIC33F family.

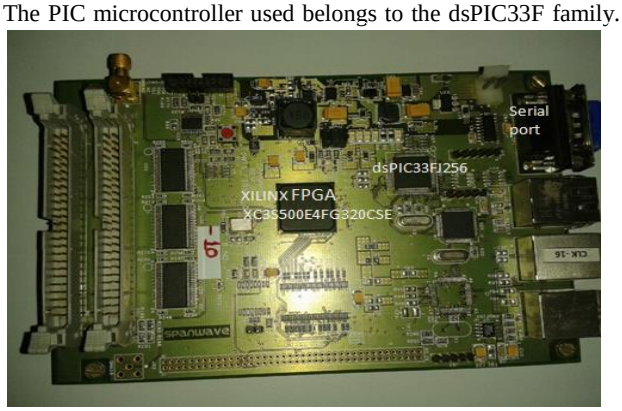

Fig.6.1: Printed Circuit Board

Through the GUI the input parameters are sent to the PCB board by PIC microcontroller using serial communication, which is in turn sent to FPGA. The FPGA then sends control signals to the 4 DDS channels as per requirement. When the AD9910 is programmed to modulate any of the DDS signal control parameters, the maximum modulation sample rate is ¼ f_{SYSCLK}. This means that the modulation signal exhibits images at multiples of ¼ f_{SYSCLK}.

The Exciter card needs waveform information and tuning word from the PC. These are downloaded into the FPGA using SPI. On the FPGA there is a UART and state machines to control the writing and reading of the necessary information. The Trigger and EPRI_Reset timing signals are generated by the timing generator using downloaded control parameters. The DDS chips are Analog Devices' AD9910. The internal RAM is used for amplitude shaping (for pulsed compressed side-lobe reduction). The internal registers are set for the chirp parameters (rate, start / stop frequency) and the internal digital ramp generator is used to make the linearly increasing chirp. The DDS trigger (IO_Update) is derived from the PRF Trigger. This is done by delaying the trigger by a set amount of time, then triggering the IO_Update on the DDS chips.

The DDS control information is of two ways, static and dynamic. Static settings are downloaded in a byte-banged software mode when the radar is started. Byte-bang is the process where the software writes a byte, and the FPGA serializes it for the DDS chips. An example of static settings is the DDS Amplitude RAM and other settings that don't change in the DDS chip. Dynamic settings are the settings inside the DDS that change on a waveform by waveform basis. When a PRF trigger occurs, the DDS is quickly loaded with the settings it needs and at the appropriate time the IO_Update line is strobed. These settings will include start frequency and start phase, amongst others. For statics settings each DDS channel is independently programmed, or can all be programmed at once. Dynamic settings are completely channel dependent, and are compiled in the radar software and downloaded into a "Serial Pattern RAM". On a trigger, a certain amount of that RAM is "played" which creates the necessary serial inputs to the DDS.

7. EXPERIMENTAL RESULTS

The Direct Digital Synthesizer is programmed with the Xilinx FPGA through SPI by using a PC interface to generate multiple radar waveforms. A 10 MHz is given from an external source to the exciter card; the clock divider AD 9520 multiplies the signal to generate 1 GHz which is fed to the DDS AD 9910.

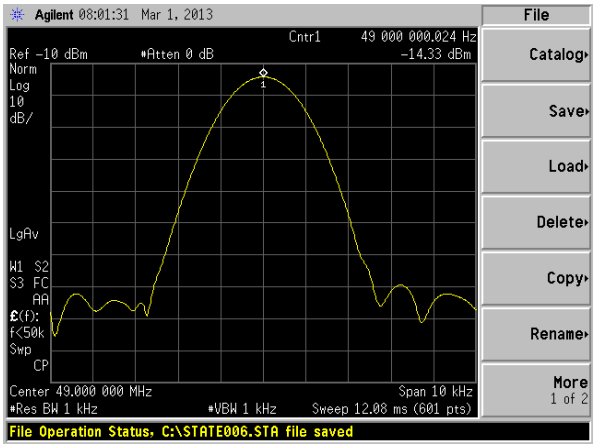

Fig 7.1: Output Waveform of 49 MHz

The AD9910 employs continuous and pulsed waveform to generate the VHF frequency of 49 MHz signal with reduces side lobes. The AD 9910 also generates a stable 35 MHz signal and 64 MHz waveform. The output resulting waveforms are shown in Fig 4.1, Fig 4.2 and Fig 4.3. The spectrum analyzer output for 35MHz signal is shown in Fig.7.1. The marker one denotes the 35MHz frequency signal with amplitude of -14.27 dBm.

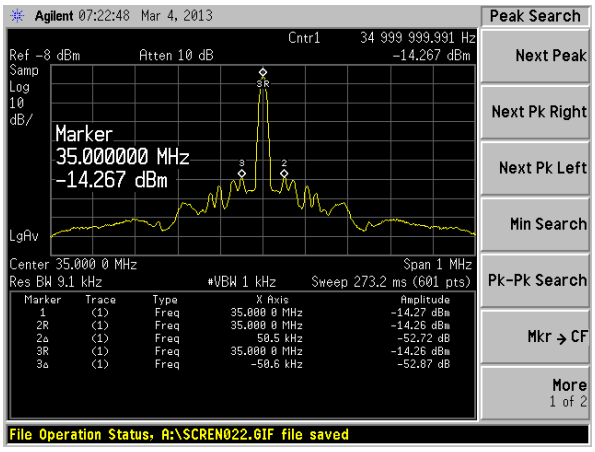

Fig 7.2: output waveform of 35 MHz

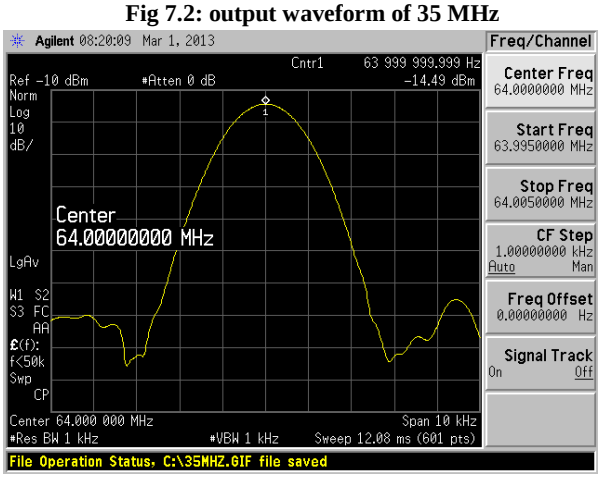

Fig 7.3: Output waveform of 64 MHz

8. CONCLUSION

In this work, we propose a method develop a RF exciter card which uses Direct Digital Synthesizer chips to generate a multi channel VHF radar frequencies for the wind profilers. With the idea of implementing an advanced technology, design of DDS based RF waveform generator was demonstrated using the XILINX FPGA and MPLAB IDE. The combination of PIC microcontroller and FPGA results in a more stable and durable RF signal generator. Using the DDS chips AD9910, we have generated the VHF frequencies of 35MHz, 49MHz and 64MHz for wind profilers.

The advantages that make high-performance, functionally integrated DDS ICs attractive to design engineers are fine tunable resolution up to 0.23Hz, sub-degree phase tuning capability, extremely fast hopping speed, fast switching and settling time and low phase noise and spurious noise. Thus the DDS based RF waveform generator developed has enormous potential to be used for the wind profilers to provide real time wind velocities which is helpful for the launch vehicles, air traffic controller, climate monitoring and in providing wind velocity data for aircrafts.

With the available time and the facilities provided, we would complete the project as required. This project is done using one board of 4 DDS chips and it can also be further implemented using 16 DDS chips (that is 4 boards with 4 DDS chips each). This project is done using AD9910 DDS chip. For further improvement of resolution, AD9912 or other DDS chips can be used. FPGA design can be implemented to ASICs and the power consumed will be reduced further. The advanced DAC chips that operate at the very high speed can be implemented into the DDS chip design.

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