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Design & Performance Analysis of Leakage Power Reduction in 6T SRAM using LECTOR & Power Gating techniques

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Abstract: In CMOS circuits, scaling of threshold voltage results in increase of sub-threshold leakage current. LECTOR is a technique for designing CMOS gates in order to reduce the leakage current without affecting the dynamic power dissipation. In this paper, I have designed the 6T SRAM cell using LECTOR based leakage reduction techniques and compare it with existing Power gating leakage reduction technique and standard CMOS technology. LECTOR technique use one extra Pull Up and Pull Down transistor in the path of V_{dd} to G_{nd} and reduce tremendous leakage current and thus reduce leakage power in CMOS circuits. I have mentioned the performance analysis in terms of Leakage Power for both Power gating and LECTOR technique with CMOS technology.

Index Terms –LECTOR, low leakage power, SRAM, Power gating, nmos, pmos

I. INTRODUCTION

The SRAM IC design consists of SRAM cells, precharge, sense amplifiers, mux, NAND gates, AND gates, NOR gates and row decoder. The most important part is the cell as all the other circuitry is connected to and around the cell. The popular, full CMOS6-transistor cell configuration was used to design the SRAM memory array. In this paper, I have designed the low power 6T SRAM cell by using two leakage control technique i.e. LECTOR and Power Gating and

A. Leakage power in SRAM

An SRAM cell is in the inactive state, when the word line is held low and bit line is charged to VDD. These inactive states come in between read and write operations. In the inactive state, different transistors dissipate leakage power depending on the value stored in the cell. This leakage current primarily owes its origin to two dominant leakage mechanism viz., sub-threshold leakage and gate leakage. Major contributors to the gate leakage current are gate oxide tunneling and injection of hot carrier from substrate to the gate oxide. Gate-induced drain leakage (GIDL) is another significant leakage mechanism, resulting due to the depletion at the drain surface below the gate-drain overlap region. Due to the substantial increase in the leakage current, the static power consumption is expected to exceed the switching component of the power consumption unless effective measures are taken to reduce the leakage power. Subthreshold leakage is the drain-source current of a transistor when the gate-source voltage is less than the threshold voltage. The subthreshold and gate tunneling leakage currents of an SRAM cell storing "0" are shown in Figure 3.3[22].More precisely, sub threshold leakage happens when the transistor is operating in the weak inversion region. The sub threshold current depends exponentially on threshold voltage, which results in large sub threshold current in short channel devices.

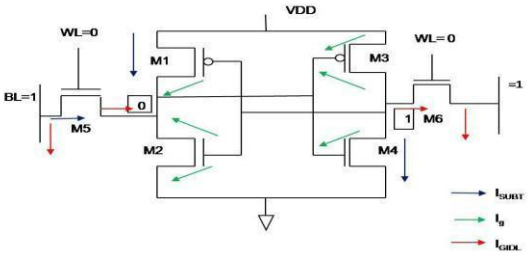

Figure 1 Schematic visualizing leakage in 6T-SRAM in standby Mode [4]

B. LECTOR technique

Two leakage control transistors (a p-type and an n-type) are introduced within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. In this arrangement, one of the LCTs is always "near its cutoff voltage" for any input combination. This increases the resistance of the path from V_{dd} to ground, leading to significant decrease in leakage currents. This is based on the observation that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path."[5]

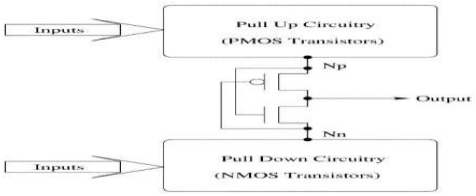

Figure 2 LECTOR technique in CMOS[4]

C. Power Gating

"The basic strategy of power gating is to provide two power modes: a low power mode and an active mode. The goal is to switch between these modes at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance."In the power gating, sleep transistors are used as switches to shut off power to parts of a design in standby mode. The header switch is implemented by pmos to control V_{dd} supply. PMOS transistor is less leaky than nmos transistor of the same size. The disadvantage of the header switch is that pmos has lower drive current than nmos of a same size. As a result, a header switch

implementation usually consumes more area than a footer switch implementation. The footer switch is implemented by nmos transistor to control V_{SS} supply. The advantage of footer switch is the high drive and hence smaller area. However, nmos is leakier than pmos and sleep transistor become more sensitive to ground noise.

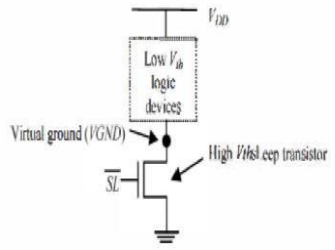

Figure 3 Power Gating in CMOS circuits using Footer switch[1]

II. EXPERIMENTAL RESULTS AND SIMULATION

A. Design of 6T SRAM cell

We are using 6 T SRAM cell type for this module. The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors. When the cell is not addressed, the two access transistors are closed and the data is kept to a stable state, latched within the flip-flop. The flip-flop needs the power supply to keep the information. The data in an SRAM cell is volatile (i.e., the data is lost when the power is removed). However, the data does not "leak away" like in a DRAM, so the SRAM does not require a refresh cycle. Static RAM is fast because the six-transistor configuration of its flip-flop circuits keeps current flowing in one direction or the other (0 or 1). Design of 6 T SRAM cell by using CMOS, LECTOR and PG has used and leakage power has been calculated.

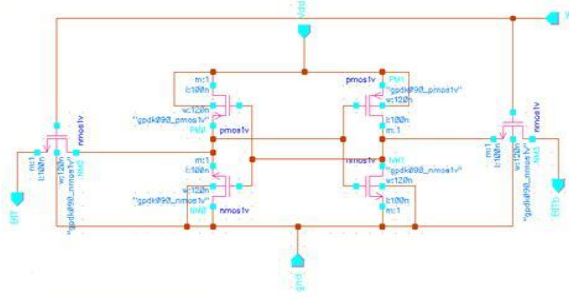

Figure 4 Schematic of 6T CMOS SRAM cell

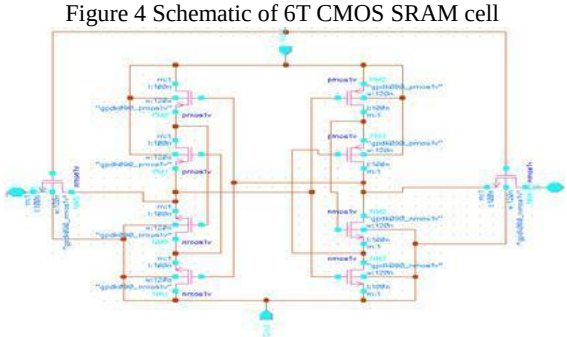

Figure 5 Schematic of 6T LECTOR SRAM cell

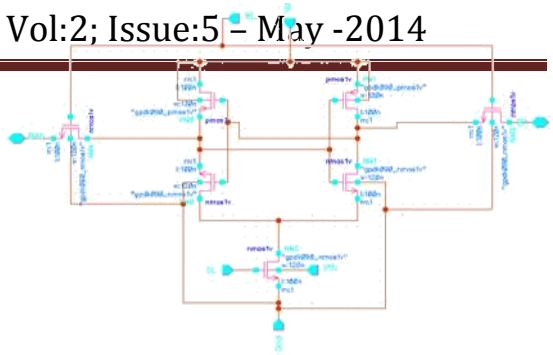

Figure 6 Schematic of 6T PG SRAM cell

B. Performance Analysis of Leakage Power in 6T SRAM

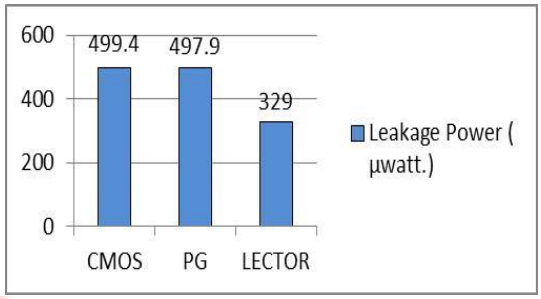

Figure 7 Leakage Power in SRAM cell

III. CONCLUSION

This paper presents a thorough analysis of LECTOR based 6T SRAM cell and compares it with Power gating structure. The key finding of the analysis is that the leakage power dissipation decreases as the stacking of transistor increases.

From the experimental results it can be verified that we get an average saving of up to 34% for leakage power reduction with using LECTOR technique if compared to Power gating and standard CMOS.

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