

FPGA Implementation of Computationally less complex BMU in Viterbi decoder for Wireless Communication system

Bhavana M
PG student,
AMCEC, Bangalore
bhavanam47@gmail.com

Mrs. Rekha Pillai
Asst.Prof, Dept of E&C,
AMCEC, Bangalore
niyathi.pillay@gmail.com

Abstract: In communication system, the wireless channels are affected by noise, attenuation, distortion and interference which affects the receiver's ability to receive correct data. This project describes the Forward Error Correction Technique (FEC) used at channel in the wireless communication system. The use of FEC technique is to increase the reliability and efficiency of digital communication and to improve the capacity of the channel. Convolutional encoder with Viterbi decoder at the receiver has been predominant FEC technique because of its high efficiency and robustness. The Viterbi decoder consists of 3-main units namely, Branch Metric Unit (BMU), Path Metric Unit (PMU) and Trace Back Unit (TBU). The conventional Viterbi algorithm used in BMU consumes more power with extra circuitry, hence in this project; the simplified algorithm is discussed to manipulate the original Viterbi algorithm used in BMU functional unit. It consumes less power and performs faster than compare to conventional method. The main aim of this paper is to implement the Convolutional encoder with constraint length $L=7$, Code rate= $1/2$ and the Soft Decision Viterbi Decoder having 64 states which decodes the original information bits for wireless communication system and is simulated on ModelsimSE6.3f and implemented using Verilog code.

Keywords : Convolutional Encoder; Viterbi Decoder; Soft decision viterbi decoder; BMU

1. INTRODUCTION

Convolutional codes were first mentioned by Elias in 1955. They can be seen as an attempt to generate the random codes that were successfully used by Shannon. Convolutional encoding is a FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by Additive White Gaussian Noise (AWGN)[1]. The information source are first convoluted and then transmitted over a noisy channel by adding proper redundancy bits to the original information bits, hence it improves the data capacity of the channel. The convolutional encoder provides powerful error correcting and encoding capability. The performance of a convolutional code depends on the coding rate and the constraint length

Andrew J. Viterbi, a founder of Qualcomm Corporation developed the viterbi decoding technique. Viterbi decoders are implementation of the Viterbi Algorithm (VA) used for

decoding of convolutional codes. A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using a Convolution code. There are other algorithms for decoding a convolutional encoded stream (for example, Fano algorithm). The Viterbi algorithm is one of the most resource-consuming algorithm, but it does the maximum likelihood decoding than others and gives reliable communication [3].

2. CONVOLUTIONAL ENCODER

Convolution encoder [1][2] is a forward error correction unit which adds proper redundancy bits to the original information bits in order to increase the channel capacity signal to noise ratio (SNR). The figure 4 shows the Convolutional encoder specified by (m, k, n) , for each clock cycle, with m -memory stages, takes one message symbol of k -bits and produces one code symbol of n bits. Convolutional codes are generated by the convolution of message sequence with set of generator polynomial sequences (G_1, G_2) . Figure below shows convolution encoder of a $(6, 1, 2)$ and g_1 and g_2 are 171o and 133o respectively.

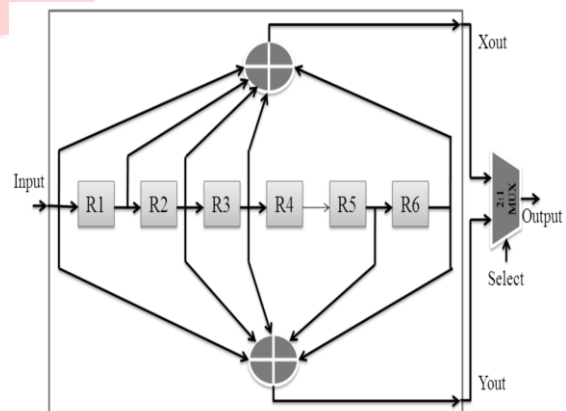


Figure1. Convolutional encoder

$G_1=1+x^1+x^2+x^3+x^6$; $Xout=171o$;

$G_2=1+x^2+x^3+x^5+x^6$; $Yout=133o$;

The code rate, $r=k/n=1/2$; expressed as a ratio of the number of input bits (k) to Convolutional encoder to the number output bits (n) of Convolutional encoder in an encoder cycle. The constraint length, $L=7$; denotes the 'Length' of the Convolutional encoder.

Convolutional encoder requires modulo-2 adders and a multiplexer in order to serialize the encoded outputs. The mod-2 adder is implemented by EXCLUSIVE-OR gate and linear addition is performed, hence the encoder is a linear feed forward shift register.

3. VITERBI DECODER

Viterbi decoding is one of two types of decoding algorithms used with convolutional encoding-the other type is sequential decoding [3]. Sequential decoding has the advantage that it can perform very well with long-constraint-length convolutional codes, but the decoding time is a variable. Viterbi decoding has the advantage that it has a fixed decoding time and it is well suited to hardware decoder implementation. But its computational requirements increases exponentially as a function of the constraint length.

By using the minimum likelihood algorithm, the Viterbi decoder core is able to correct errors in received data caused by channel noise. The decoded output data is equivalent to the transmitted digital data stream. Viterbi Decoders can be classified into two types

with the higher metric value is discarded and the one with the lower metric value is kept. The path selected are called survivors path.

Soft decision Viterbi decoder quantizes the received noisy signal into multiple levels, which results in high accuracy for predicting encoded data. Soft decision Viterbi Decoder consist of 3 units to decode the received noisy signal as shown in Figure 3; they are

- Branch Metric Unit
- Path Metric Unit
- Trace Back Unit

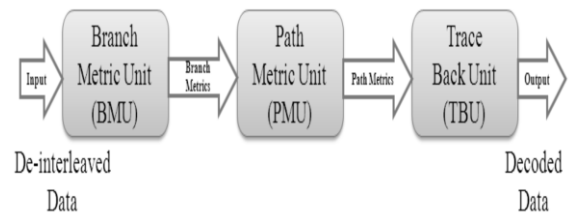


Figure 3. Viterbi decoder

3.1 HARD VITERBI DECODER

Hard decision Viterbi decoder quantizes the received noisy signal into two levels only, either 0 or 1, which results in less accuracy for predicting encoded data hence results in increased bit error rate.

3.2 SOFT VITERBI DECODER

Soft Decision Viterbi decoder implements the Viterbi algorithm[4][5], Viterbi algorithm detects the most likely transmitted signal by using trellis structure, trellis structure consist of states and branches as shown in Figure 2 for constraint length 3.

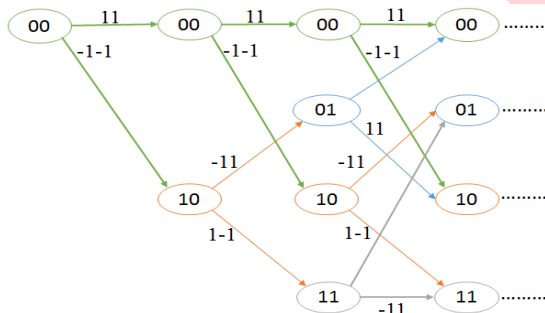


Figure 2. Trellis structure for constraint length 3

Branches indicates the probable transitions from one state to another with weight as distance between received signal and actual output of encoder while traversing from one state to another state, maximum number of states at each stage is 2^k where k is the number of memory elements used in the Convolutional encoder.

The Viterbi decoder examines the received data sequence. Then computes a branch metric for each path and makes the decision based on the branch metric values. All paths are followed until 2-paths converge on one node. Then the path

3.3 BRANCH METRIC UNIT

3.3.1 Euclidean approach for Branch Metric Unit

The branch metric unit computes $2^n = 4$ branch metrics for a set of $n=2$. The first step in Viterbi decoder is to find Euclidian distance - the squared distance between the received noisy symbol and the ideal output symbol. This distance is known as Branch metric.

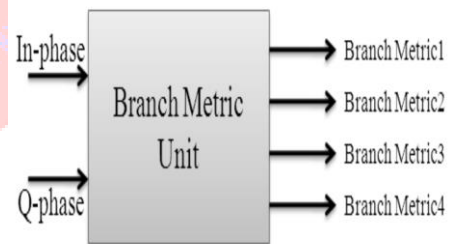


Figure 4. Branch metric unit

The figure 4 shows the BMU's inputs and the outputs. The inputs are the quantized noisy signal and the outputs are the Branch metrics calculated for all the 4 original QPSK signals. The distance (d) between the received signal and the ideal QPSK on the constellation diagram is calculated by the Euclidean distance formula given below in the equation (1) and its expansion is given in equation (2).

$$\text{BMU Euclidean } [r, i] = (r-r_0)^2 + (i-i_0)^2 \quad (1)$$

$$\text{BMU} = (r^2 - 2*r*r_0 + r_0^2) + (i^2 - 2*i*i_0 + i_0^2) \quad (2)$$

Where r, i are real and imaginary components

r=received signal value of real part

r0= ideal value of real part

i= received signal value of imaginary part

$i0$ = ideal value of imaginary part

As the above Euclidean is a conventional method, it requires 8 multipliers and 4 summations functional unit for each computation, hence it consumes more area and power hence the absolute method is as followed.

3.3.2 Absolute approach for Branch Metric Unit

By cancelling the squared terms of r and i , the equation (2) is reduced to equation (3) which requires only 2 multipliers, hence it consumes less area and power compare to Euclidean approach. The distance is found by the following simplified Equation (3). Since I_i and I_q are ideal values it may be ± 1 .

$$\text{BMUAbsolute} = -(\pm r) - (\pm i) \quad (3)$$

Where (r, i) is the received symbol, \pm indicates ideal transmitted symbols $+$ for 0 and $-$ for 1. Hence the Absolute method requires 1 multipliers and 1 summations functional unit for each computations. Hence this absolute approach gives the same results by utilizing less hardware and less power compared to Euclidean distance measure. The synthesis of BMU using both approaches is carried out.

Table.1 and Table.2 shows the device utilization summary of the BMU using Euclidean Distance approach and Absolute approach respectively. It indicates that the area taken by BMU using Euclidean Distance approach is 80% more than the area taken by BMU using Absolute approach, hence results in low power consumption using Absolute approach.

Table1: Device utilization summary for Euclidean approach

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	25	69120	0%
Number of Slice LUTs	34	69120	0%
Number of fully used LUTFF pairs	13	41	43%
Number of bonded I/OBs	30	640	4%
Number of BUFGs/BUFGCTRLs	1	32	3%

Table 2: Device utilization summary for Absolute approach

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	23	69120	0%
Number of fully used LUTFF pairs	0	23	0%
Number of bonded I/OBs	30	640	4%
Number of BUFGs/BUFGCTRLs	1	32	3%

3.4 PATH METRIC UNIT

Path metrics are calculated using a procedure called ACS(Add-Compare-Select). This procedure must be repeated for every encoder state and gives the minimum path metric(survivor path) for each state metric. The ACS module is shown in Figure 5.

3.4.1 Add

For a given state, there will be two states on the previous step which can move to this State and the output bit pairs that correspond to these transitions. In order to calculate new path Metrics, we must add the previous path metrics with the corresponding branch metrics.

3.4.2 Compare, select

There are two paths, ending in a given state. One of them with greater path metric is dropped. The above steps are repeated for every symbol.

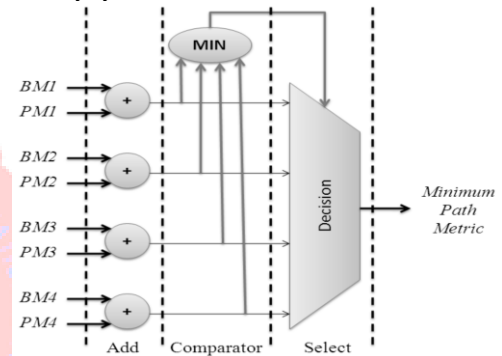


Figure 5. Add-Compare-Select unit

3.5 TRACE BACK UNIT

The TBU extracts the decoded bits, when all the path metrics (survivor paths) computations are completed, the trace back unit searches for the maximum likelihood path from end of the survivor paths to the beginning and provides the maximum likelihood decoded bits.

4. SIMULATION RESULTS FOR CONVOLUTIONAL ENCODER AND VITERBI DECODER

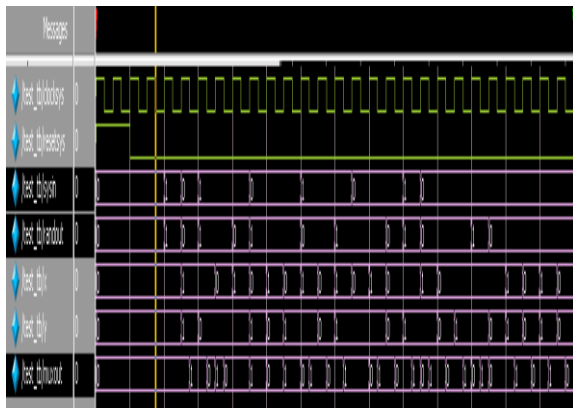


Figure. 6 Waveform screenshot of software simulation for Convolutional Encoder

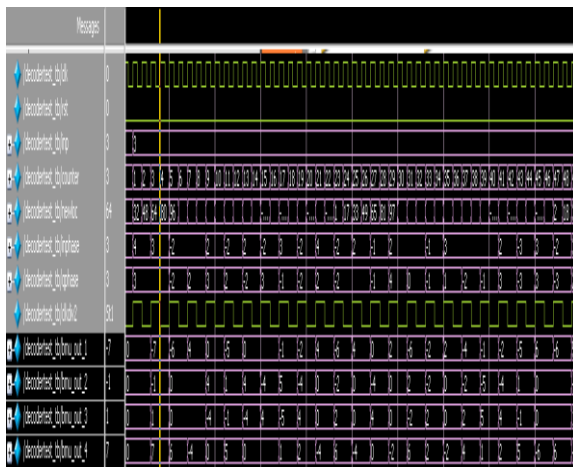


Figure.7 Branch metric calculation results using absolute approach

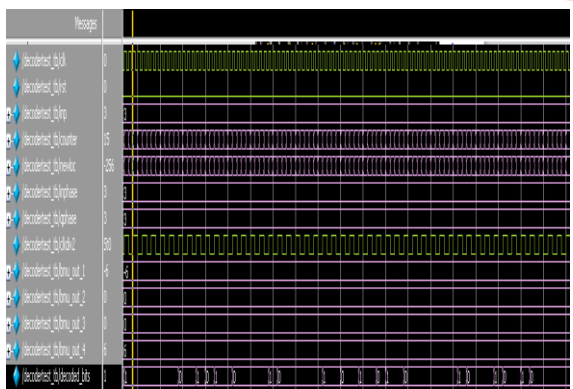


Figure.8 Waveform screenshot of software simulation for soft decision Viterbi Decoder

CONCLUSIONS

In this paper, we present an implementation of both convolutional encoder with a constraint length of 7 and a code rate of 1/2 and soft decision Viterbi decoder on FPGA to reduce the bit error rate. The presented paper describes

about the channel encoding and decoding method. The combination of convolution encoder and Viterbi decoder has been widely used in cell phones, broadband internet, etc. because of its low bit error rate between the transmission and reception.

The soft decision Viterbi offers high accuracy in prediction the encoded data by convolution encoded bits, hence reduces the BER and improves the reliability and efficiency of the digital communication System than the Hard Decision Viterbi decoder. The new simplified absolute method consumes less power than the original method which uses Euclidean distance formula to calculate the Branch metrics in the Branch metric unit of the Viterbi decoder. Thus, the Viterbi decoder consuming less area and low power is achieved compared to Euclidean approach.

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